AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A processor, comprising:

a first register configured to store one or more ~~hardware debug test (HDT)~~ enable bits for a hardware debugging mode;

a first control logic coupled to receive a plurality of [[HDT]] input signals associated with the hardware debugging mode, wherein the first control logic is coupled to access the first register; and

a second control logic coupled to the first register, wherein the second control logic is configured to store one or more default values in the first register in response to a reset of the processor.

2. (Currently Amended) The processor of claim 1, wherein the first control logic is further configured to receive a request to enter the hardware debugging ~~an HDT~~ mode, wherein the first control logic is further configured to read selected entries of the one or more [[HDT]] enable bits stored in the first register in response to the request to enter the hardware debugging ~~HDT~~ mode, and wherein the first control logic is further configured to grant or deny the request to enter the hardware debugging ~~HDT~~ mode based on the selected entries of the one or more [[HDT]] enable bits.

3. (Currently Amended) The processor of claim 1, further comprising:

one or more non-volatile memory cells configured to store the one or more default values for the one or more [[HDT]] enable bits.

4. (Currently Amended) The processor of claim 3, wherein the second control logic is further coupled to read the one or more default values for the one or more [[HDT]] enable bits from the one or more non-volatile memory cells and to write the one or more default values for the one or more [[HDT]] enable bits into the first register in response to the reset of the processor.

5. (Currently Amended) The processor of claim 1, wherein the second control logic is further coupled to receive a signal indicative of the one or more default values for the one or more [[HDT]] enable bits and to write the one or more default values for the one or more [[HDT]] enable bits into the first register in response to the reset of the processor.

6. (Original) The processor of claim 1, wherein the second control logic is coupled to receive a RESET signal in response to the reset of the processor.

7. (Original) The processor of claim 1, further comprising:

a third register configured to store one or more microcode loader enable bits;

a third control logic coupled to receive a plurality of microcode inputs, wherein the third control logic is coupled to access the third register; and

a fourth control logic coupled to the third register, wherein the fourth control logic is configured to store one or more default values in the third register in response to a reset of the processor.

8. (Original) The processor of claim 7, wherein the third control logic is further configured to receive a request to modify microcode, wherein the third control logic is further configured to read selected entries of the one or more microcode loader enable bits stored in the third register in response to the request to modify microcode, and wherein the third control logic is further configured to grant or deny the request to modify microcode based on the selected entries of the one or more microcode loader enable bits.

9. (Currently Amended) The processor of claim 1, further comprising:

a second register coupled to the first control logic, wherein the second register is configured to store one or more [[HDT]] enable lock bits.

10. (Currently Amended) The processor of claim 9, wherein the first control logic is further configured to receive a request to modify the hardware debugging ~~HDT~~ mode status, wherein the first control logic is further configured to read selected entries in the one or more [[HDT]] enable lock bits stored in the second register in response to the request to modify the hardware debugging ~~HDT~~ mode status, and wherein the first control logic is further configured to grant or deny the request to modify the hardware debugging ~~HDT~~ mode based on the selected entries in the one or more [[HDT]] enable lock bits.

11. (Currently Amended) The processor of claim 9, wherein the first register and the second register are unified into a single register configured to store two or more bits, including one or more [[HDT]] enable bits and one or more [[HDT]] enable lock bits.

12. (Original) The processor of claim 9, further comprising:

a third register configured to store one or more microcode loader enable bits;

a third control logic coupled to receive a plurality of microcode inputs, wherein the third control logic is coupled to access the third register; and

a fourth control logic coupled to the third register, wherein the fourth control logic is configured to store one or more default values in the third register in response to a reset of the processor.

13. (Original) The processor of claim 12, wherein the third control logic is further configured to receive a request to modify microcode, wherein the third control logic is further configured to read selected entries in the one or more microcode loader enable bits stored in the third register in response to the request to modify microcode, and wherein the third control logic is further configured to grant or deny the request to modify microcode based on the selected entries in the one or more microcode loader enable bits.

14. (Original) The processor of claim 12, wherein the second and fourth control logics are unified.

15. (Original) The processor of claim 14, wherein the first control logic, the second control logic, the third control logic, and the fourth control logic are unified.

16-34. (Canceled)

35. (Currently Amended) A method of operating a processor, the method comprising:

obtaining one or more default values, wherein obtaining the one or more default values is selected from the group consisting of:

reading the one or more default values from one or more non-volatile memory cells, and

receiving the one or more default values as a strapped value through a pull-up or pull-down resistor; and

writing the one or more default values as one or more various entries in one or more registers in response to a reset of the processor, wherein the one or more various entries are selected from the group consisting of:

one or more [[HDT]] enable bits associated with a hardware debugging mode,

one or more [[HDT]] enable lock bits associated with the enable bits,

one or more microcode loader enable bits, and

one or more microcode loader enable lock bits.

36-40. (Canceled)

41. (Currently Amended) A processor, comprising:

means for storing one or more default values, wherein the default values are selected from the group consisting of:

[[HDT]] enable status associated with a hardware debugging mode,

[[HDT]] enable lock status associated with the enable status,

microcode loader enable status, and

microcode loader enable lock status;

means for obtaining the one or more default values, wherein obtaining the one or more default values is selected from the group consisting of:

reading the one or more default values from non-volatile memory, and

receiving the one or more default values as a strapped value through a pull-up or pull-down resistor; and

means for writing the one or more default values as one or more various entries in the means for storing the one or more default values in response to a reset of the processor, wherein the one or more various entries are selected from the group consisting of:

one or more [[HDT]] enable bits associated with the hardware debugging mode,

one or more [[HDT]] enable lock bits associated with the enable bits,

one or more microcode loader enable bits, and

one or more microcode loader enable lock bits.

42. (Currently Amended) A computer system, comprising:

a processor, comprising:

means for storing one or more default values, wherein the default values are selected from the group consisting of:

[[HDT]] enable status associated with a hardware debugging mode,

[[HDT]] enable lock status associated with the enable status,

microcode loader enable status, and

microcode loader enable lock status;

means for obtaining the one or more default values, wherein obtaining the one or more default values is selected from the group consisting of:

reading the one or more default values from non-volatile memory, and

receiving the one or more default values as a strapped value through a pull-up or pull-down resistor; and

means for writing the one or more default values as one or more various entries in the means for storing the one or more default values in response to a reset of the processor, wherein the one or more various entries are selected from the group consisting of:

one or more [[HDT]] enable bits associated with the hardware debugging mode,

one or more [[HDT]] enable lock bits associated with the enable bits,

one or more microcode loader enable bits, and

one or more microcode loader enable lock bits;

a bridge coupled to the processor; and

a memory operably coupled to the processor, wherein the memory is configured to store BIOS code.

43-52. (Canceled)

53. (Currently Amended) A computer readable program storage device encoded with instructions that, when executed by a computer system, performs a method of operating a processor, the method comprising:

obtaining one or more default values, wherein obtaining the one or more default values is selected from the group consisting of:

reading the one or more default values from one or more non-volatile memory cells, and

receiving the one or more default values as a strapped value through a pull-up or pull-down resistor; and

writing the one or more default values as one or more various entries in one or more registers in response to a reset of the processor, wherein the one or more various entries are selected from the group consisting of:

one or more [[HDT]] enable bits associated with the hardware debugging mode,

one or more [[HDT]] enable lock bits associated with the enable bits,

one or more microcode loader enable bits, and

one or more microcode loader enable lock bits.